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CITATION:

Funaki, Tsuyoshi ...[et al]. Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices. IEEE TRANSACTIONS ON POWER ELECTRONICS 2009, 24(5-6): 1486-1493

ISSUE DATE:

2009-05

URL:

http://hdl.handle.net/2433/109805

Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices

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***Abstract*—The switching behavior of semiconductor devices responds to charge/discharge phenomenon of terminal capacitance in the device. The differential capacitance in a semiconductor device varies with the applied voltage in accordance with the depleted region thickness. This study develops a C–V characterization system for high-voltage power transistors (e.g., MOSFET, insulated gate bipolar transistor, and JFET), which realizes the selective measurement of a specified capacitance from among several capacitances integrated in one device. Three capacitances between terminals are evaluated to specify device characteristics—the capacitance for gate–source, gate–drain, and drain–source. The input, output, and reverse transfer capacitance are also evaluated to assess the switching behavior of the power transistor in the circuit. Thus, this paper discusses the five specifications of a C–V characterization system and its measurement results. Moreover, the developed C–V characterization system enables measurement of the transistor capacitances from its blocking condition to the conducting condition with a varying gate bias voltage. The measured C–V characteristics show intricate changes in the low-bias-voltage region, which reflect the device structure. The monotonic capacitance change in the high-voltage region is attributable to the expansion of the depletion region in the drift region. These results help to understand the dynamic behavior of high-power devices during switching operation.**

***Index Terms*—C–V characteristics, high-voltage power device, terminal capacitance, voltage dependency.**

I. Introduction

POWER electronics requires high efficiency and versatile power conversion. High-voltage capability is preferable, especially in high-power circuits, to reduce the conduction loss of large currents. High-frequency switching enables minimization of bulky passive components and provides control functionality. The power switching device is the key component in realizing this; therefore, development efforts focus on a power device with a high breakdown voltage, low forward voltage drop, and fast switching capability [1]–[3].

As a result, an Si-insulated gate bipolar transistor (IGBT) has been developed and improved to meet these requirements [4], [5]. Recently, a superjunction structure of Si power MOSFET was proposed to realize a high breakdown voltage using a p-n junction and fast switching capability by majority carriers [6]–[8]. In addition to the Si-based power device, wide-bandgap semiconductor power devices have been researched and developed to realize lower loss, higher voltage breakdown, and faster switching with a thin voltage blocking layer. SiC and GaN devices are good examples [3], [7], [9]–[21].

The capacitance between the terminals of a power device affects its switching behavior, because it must be charged and discharged during turn-off and turn-on operations [22], [23]. The capacitance of a power device increases as the thickness of the voltage blocking layer is decreased to minimize conduction resistance. The capacitance varies widely with the applied bias voltage because of depletion in the voltage blocking layer. Therefore, it is necessary to quantify the capacitance between the terminals of the power device as well as the capacitance's voltage dependency. One method is to estimate the capacitance value with finite-element (FE) device simulation and validate it with circuit simulation or experiments [24]–[26]. However, this approach requires a detailed device structure, dimensions, and process parameters. Another method is to characterize the capacitances experimentally. However, there is no commercial product that is able to measure the terminal capacitance of a high-voltage power device by applying the bias voltage up to its rated value. JEDEC [27] and IEC [28] standardized the capacitance measurement between the terminals of a power device with a capacitance bridge, but no actual configuration or circuit topology for the measurements are provided. Elferich *et al*. [26] measured the C–V characteristics of a power MOSFET and validated the FE device simulation; however, the measurement setup is not clearly described and the applied voltage was low ($0 \leq V_{\rm ds} \leq 20, -10 \leq V_{\rm gs} \leq 0$). Therefore, the authors developed a C–V measurement system for high-voltage power devices. Funaki *et al.* [29] and [30] presented the C–V measurement system for high-voltage power diodes with evolving [31] and clarified the punch-through structure of SiC Schottky barrier diodes (SBDs) from the measured results. This study develops a C–V measurement system for gate-controlled, high-voltage

Manuscript received October 1, 2008; revised February 21, 2009. Current version published May 29, 2009. This work was supported in part by the Ministry of Education, Culture, Sports, Sciences and Technology in Japan, under Grant-in-Aid for Scientific Research 17686024, Grant 18360137, and the 21st Century Centers of Excellence (COE) Program 14213201. Recommended for publication by Associate Editor J. Shen.

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Digital Object Identifier 10.1109/TPEL.2009.2016566

power devices, e.g., power MOSFET, JFET, and IGBT. There are three terminals in a single device, and five specifications of the measurement circuit are presented to measure the capacitance between gate–source ($C_{\rm gs}$), gate–drain ($C_{\rm gd}$), and drain–source ($C_{\rm ds}$), and to measure input ($C_{\rm iss}$), output ($C_{\rm oss}$), and reverse transfer ($C_{\rm rss} = C_{\rm gd}$) capacitances. The capacitances $C_{\rm gs}$, $C_{\rm ds}$, and $C_{\rm ds}$ are measured to clarify the device structure and physical behavior, and $C_{\rm iss}$, $C_{\rm oss}$, and $C_{\rm rss}$ are used to estimate their influence on circuit operation.

The developed measurement circuit can apply a bias voltage between drain and source, and simultaneously to the gate with reference to the source potential. Thus, the circuit can measure the C–V characteristics for both normally OFF and normally ON devices [32]. Also, it enables measurement of the capacitances from the blocking condition to the conducting condition with varying gate bias voltage. For instance, an IGBT is a high-voltage power device, and its measurements illustrate the physical phenomenon occurring in the device, which depends on the applied drain (collector) and gate bias voltage.

II. Capacitance of a Power Device and Measurement Circuit

This section examines the makeup of the capacitive component in a power transistor when assuming a planar gate device structure and a vertical drift region-type double-diffusion MOSFET (VDMOSFET) [3]. Further, the paper discusses a circuit for measuring the capacitance between the power device terminals; the circuit can apply a bias voltage between the drain and the source, and the gate and the source, up to the rated voltage of the device.

A. Terminal Capacitance of VDMOSFET

Fig. 1(a) shows the cross section of one cell in a VDMOSFET chip. The main dielectrics for inducing capacitance in the cell are the depletion layer formed in the semiconductor and the gate oxides. The capacitances arising from the gate oxide have a constant value, irrespective of the voltage applied across it. However, the capacitance arising from the depletion layer, which is formed in the semiconductor, changes with the applied voltage across it, where the capacitance is treated as a differential capacitance dQ/dV. Here, dQ denotes the charge depleted to the incremental bias voltage dV. The capacitance components that reside in the VDMOSFET are integrated into the terminal capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$, when seen from the terminal of the electrode in a discrete device, as shown in Fig. 1(b). These terminal capacitances are configured by the capacitive components shown in Fig. 1(a) as

$$\begin{cases} C_{\rm gs} = C_{\rm m} + C_{\rm oxs} + \frac{1}{1/C_{\rm oxc}+1/C_{\rm c}} \\ C_{\rm gd} = \frac{1}{1/C_{\rm oxd}+1/C_{\rm gdj}} \\ C_{\rm ds} = C_{\rm dsj}. \end{cases} \quad (1)$$

Here, C_m is the capacitance between the gate electrode and the source electrode across the gate oxide, $C_{\rm oxs}$ is the capacitance of the gate electrode and source n^+ region, $C_{\rm oxc}$ is the capacitance of the gate electrode and the top surface of the p^+ region, $C_{\rm c}$ is the capacitance of the depletion region for the p^+ region under the gate, $C_{\rm oxd}$ is the capacitance of the gate electrode and top surface of the drain region across the gate oxide, $C_{\rm gdj}$ is the capacitance of the depletion region for the drain under the gate, and $C_{\rm dsj}$ is the capacitance of the depletion region for the drain under the source.

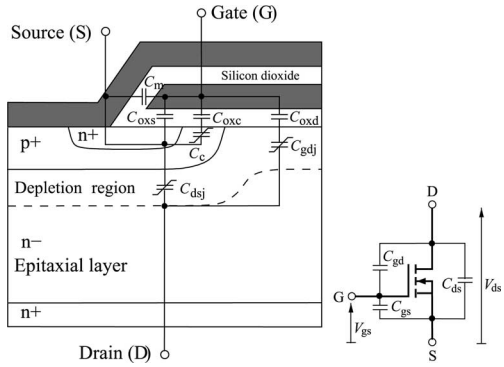

Fig. 1. Example of a gate-controlled transistor to illustrate device capacitance. (a) Cross section of a VDMOSFET cell. (b) Equivalent capacitances between terminals of VDMOSFET.

The combination of terminal capacitances in the power device determines circuit operation. The input capacitance is the equivalent capacitance when the transistor is seen from the gate terminal to drive the gate; it can be expressed as $C_{\rm iss} = C_{\rm gs} + C_{\rm gd}$. The reverse transfer capacitance ($C_{\rm rss}$) is the same as $C_{\rm gd}$. It induces the well-known Miller effect and deteriorates the gate driving response because of the effectively increased capacitance by the multiplier factor of device transconductance [22]. The output capacitance corresponds to the capacitance seen from the drain terminal, and its charge/discharge operation by the drain current affects the main circuit response. It can be expressed as $C_{\rm oss} = C_{\rm ds} + C_{\rm gd}$. Thus, five capacitance specifications are needed to characterize the device.

B. $C_{\rm gs}$ Measurement Circuit

Fig. 2 shows the circuit for measuring $C_{\rm gs}$. This circuit can perform four-terminal (Kelvin sense) measurements—$H_{\rm pot}$ and $L_{\rm pot}$ (for detecting the small ac voltage of the measurement signal) and $H_{\rm cur}$ and $L_{\rm cur}$ (for detecting the current of the measurement signal). The four measurement terminals are connected to an *LCR* meter or impedance analyzer.

$C1$ and $C2$ block the bias gate voltage, transferring only the ac measurement signal from terminals $H_{\rm pot}$ and $H_{\rm cur}$. These blocking capacitors enable application of the gate–source bias voltage ($V_{\rm gs}$), and the circuit measures the capacitance characteristics related to channel condition, such as accumulation, depletion, and inversion. Moreover, the blocking capacitance enables the measurement of $C_{\rm gs}$ for a normally ON device by applying a gate voltage and making the device channel operate in the blocking condition. The voltage source $V_{\rm gs}$ and $V_{\rm ds}$ impose the dc bias voltage, and the C–V characteristics are measured by sweeping one of them. The ac measurement signal at the source terminal is blocked by $L1$ (because of its high impedance at the operating frequency); therefore, it is transferred to terminals $L_{\rm cur}$ and $L_{\rm pot}$. $L1$ shorts the source terminal to dc ground

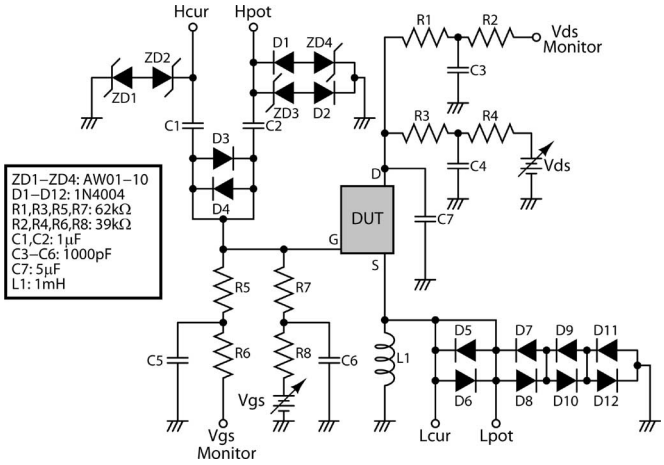

Fig. 2. $C_{\rm gs}$ measurement circuit.

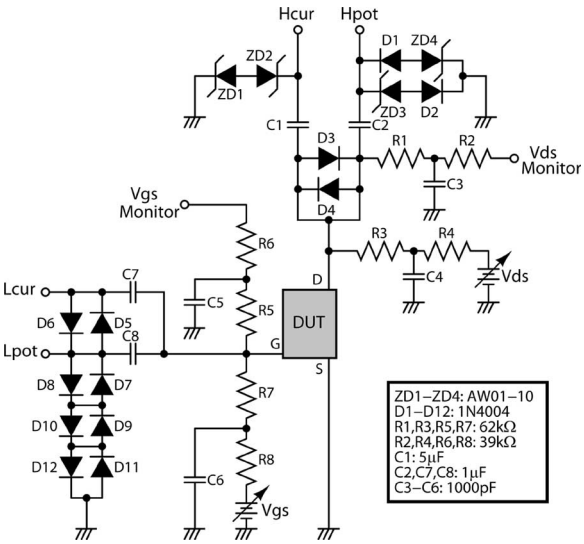

Fig. 3. $C_{\rm gd}$ $(C_{\rm rss})$ measurement circuit.

and establishes the dc bias voltages $V_{\rm gs}$ and $V_{\rm ds}$ at the device terminals with reference to ground potential. Diodes D1–D12 and ZD1–ZD4 provide protection. The *RC* circuit at the voltage source input and the monitor output constitute a low-pass filter to block the measurement signal, and apply and measure the dc bias voltage. $C7$ shorts the drain terminal when measuring an ac frequency and blocks dc from the measurement.

C. $C_{\rm gd}$ $(C_{\rm rss})$ Measurement Circuit

Fig. 3 shows the circuit diagram for measuring $C_{\rm gd}$ $(C_{\rm rss})$. This circuit has two groups of blocking capacitors for the drain and source terminals to ensure ground potential at the source terminal. $C1$ and $C2$ block the dc bias voltage of $V_{\rm ds}$, and $C7$ and $C8$ block the dc bias voltage of $V_{\rm gs}$. The capacitances transfer the ac measurement signal from $H_{\rm cur}$ and $H_{\rm pot}$ to $L_{\rm cur}$ and $L_{\rm pot}$, respectively. The source terminal is directly grounded, and the capacitance component in the device related

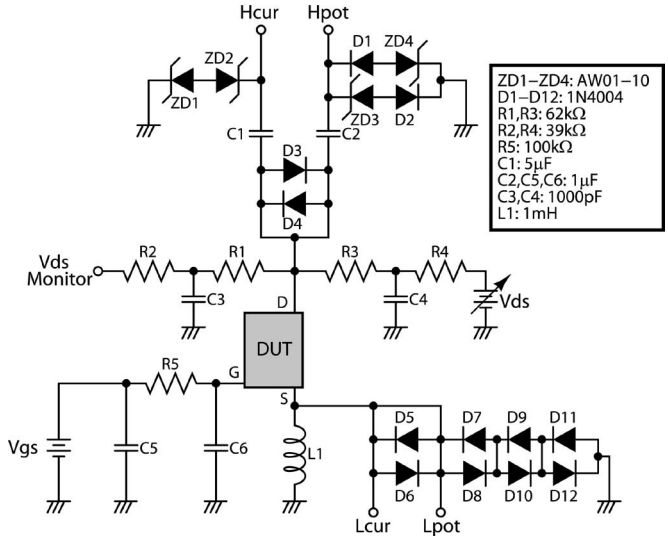

Fig. 4. $C_{\rm ds}$ measurement circuit.

to the source terminal is excluded from the measurement. The dc bias voltages $V_{\rm ds}$ and $V_{\rm gs}$ are applied and monitored through the *RC* filter.

D. $C_{\rm ds}$ Measurement Circuit

Fig. 4 shows the circuit diagram for measuring $C_{\rm ds}$. $C1$ and $C2$ block the dc bias voltage $V_{\rm ds}$ and transfer the ac measurement signal from $H_{\rm cur}$ and $H_{\rm pot}$ terminals. The dc bias voltages $V_{\rm ds}$ and $V_{\rm gs}$ are applied and monitored through the *RC* filter circuit. Inductor $L1$, connected to the source terminal, blocks the measurement ac signal and transfers it to $L_{\rm cur}$ and $L_{\rm pot}$. However, it shorts the source terminal to dc ground and helps establish the dc bias voltage with reference to the source terminal. $C6$, connected to the gate terminal, blocks the dc voltage and establishes the dc potential of the gate terminal, but shorts ac signals to ground. Therefore, the capacitive component connected to the gate terminal is excluded from the measurement since it is shunted to the ground.

E. $C_{\rm iss}$ Measurement Circuit

Fig. 5 shows the circuit diagram for measuring the input capacitance $C_{\rm iss}$. This circuit differs from the former measurement circuits in that it measures the combined capacitance of $C_{\rm gs}$ and $C_{\rm gd}$, which have different dc potentials for the drain and source. $C1$, $C2$, $C7$, and $C8$ block the dc bias voltages of $V_{\rm ds}$ and $V_{\rm gs}$, and transfer the ac measurement signal from $H_{\rm cur}$ and $H_{\rm pot}$ to $L_{\rm cur}$ and $L_{\rm pot}$, respectively. The dc bias voltages $V_{\rm ds}$ and $V_{\rm gs}$ are applied and monitored through the *RC* filter. Inductor $L1$ shorts dc signals at the source terminal to ground, establishes the reference potential for the dc bias voltage, and blocks the ac measurement signal from shorting to ground. The blocked ac measurement signal is transferred to $H_{\rm cur}$ and $H_{\rm pot}$ terminals through the bypass capacitors $C9$ and $C10$. Consequentially, the capacitance between the drain and source terminals are eliminated by bypass capacitors $C1$, $C2$, $C9$, and $C10$.

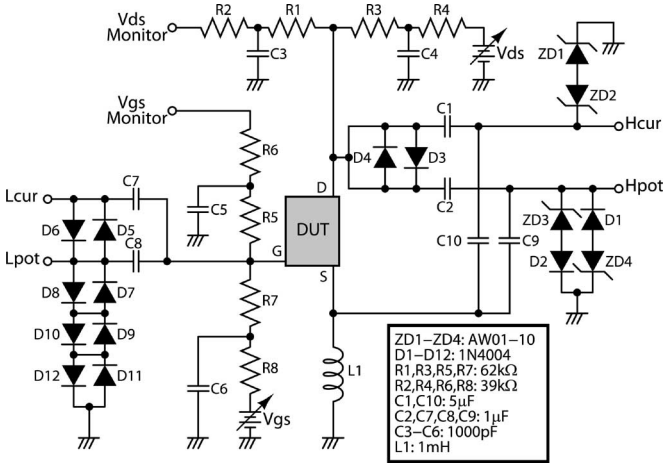

Fig. 5. $C_{\rm iss}$ measurement circuit.

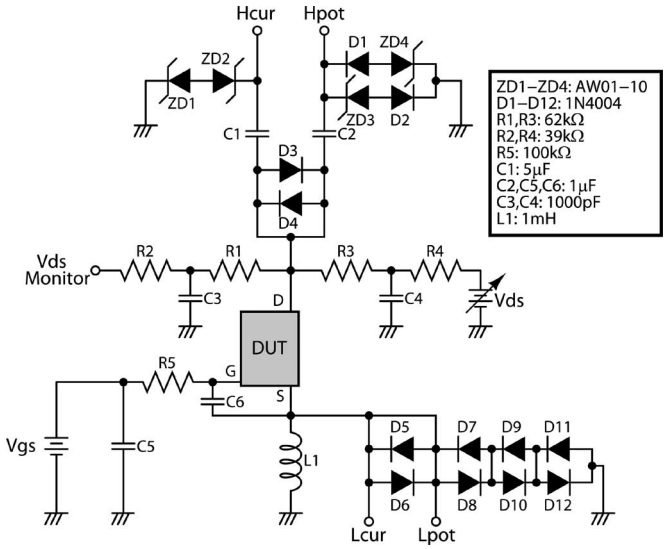

Fig. 6. $C_{\rm oss}$ measurement circuit.

F. $C_{\rm oss}$ Measurement Circuit

Fig. 6 shows the circuit diagram for measuring the output capacitance $C_{\rm oss}$, which is the combined capacitance of $C_{\rm ds}$ and $C_{\rm gd}$—the capacitances have different dc potentials at the gate and source terminals. Capacitors $C1$ and $C2$ block the dc bias voltage of $V_{\rm ds}$ and transfer the ac measurement signal from terminals $H_{\rm cur}$ and $H_{\rm pot}$. The dc bias voltages $V_{\rm ds}$ and $V_{\rm gs}$ are applied and monitored through the *RC* filter. $L1$ shorts dc signals to ground at the source terminal and establishes the reference potential for the dc bias voltage. It also blocks the ac measurement signal from shorting to ground and helps transfer it to terminals $L_{\rm cur}$ and $L_{\rm pot}$. $C6$ blocks the dc bias voltage of $V_{\rm gs}$ from the source and passes the ac measurement signal, which is then transferred to $L_{\rm cur}$ and $L_{\rm pot}$ terminals; $L1$ provides a high ac resistance to ground. $C6$ bypasses and eliminates the capacitance between the gate and source $(C_{\rm gs})$.

The values of the blocking and bypass capacitances are selected to have sufficiently small impedance relative to the capacitance measurement or elimination ability in the device.

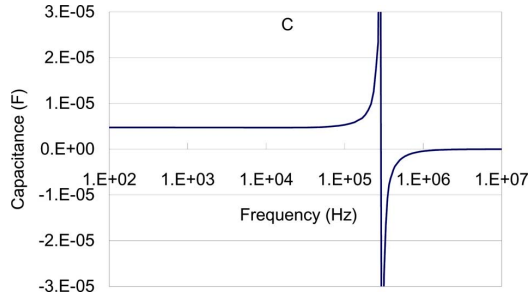

Fig. 7. Frequency characteristics of the blocking capacitor. (4.7 μF, 630 V, film-type capacitor, $C_{\rm s} + R_{\rm s}$ measurement.)

TABLE I
TEST RESULTS FOR REFERENCE CAPACITANCE (nF)

GS	GD	DS	$C_{\rm gs}$ (err%)	$C_{\rm gd}$ (err%)	$C_{\rm iss}$ (err%)	$C_{\rm gs}+C_{\rm gd}$ (err%)	$C_{\rm ds}$ (err%)	$C_{\rm oss}$ (err%)	$C_{\rm ds}+C_{\rm gd}$ (err%)
Ca	Cb	Cc	11.465 (4.104)	21.439 (0.603)	32.642 (0.184)	32.904 (0.988)	33.346 (0.036)	54.494 (0.788)	54.785 (0.259)
Ca	Cc	Cb	11.332 (2.897)	33.254 (0.312)	44.462 (0.205)	44.586 (0.485)	22.112 (2.518)	53.888 (1.892)	55.366 (0.799)
Cb	Ca	Cc	22.022 (2.100)	11.018 (0.045)	32.715 (0.408)	33.040 (1.406)	34.053 (2.083)	44.304 (0.151)	45.071 (1.578)
Cb	Cc	Ca	21.742 (0.802)	33.415 (0.171)	55.176 (0.453)	55.157 (0.419)	11.456 (4.023)	43.354 (2.292)	44.871 (1.127)
Cc	Ca	Cb	33.826 (1.403)	11.049 (0.327)	44.645 (0.618)	44.875 (1.136)	22.399 (3.848)	32.466 (0.356)	33.448 (2.658)
Cc	Cb	Ca	33.592 (0.701)	21.376 (0.895)	55.248 (0.584)	54.968 (0.075)	11.505 (4.467)	32.155 (1.311)	32.881 (0.918)

$Ca = 11.013$ nF, $Cb = 21.569$ nF, $Cc = 33.358$ nF

Film-type capacitors are adopted because of their superior high-frequency performance, but high-voltage-blocking large capacitors tend to be bulky and have relatively large effective series inductance (ESL). Fig. 7 shows the frequency characteristics of the capacitance used for blocking high voltages as measured by an impedance analyzer (Agilent 4294A). The largest capacitance used in the measurement circuit has a self-resonant frequency around 300 kHz because of the capacitance and ESL, as shown in Fig. 7. JEDEC [32] suggests that the measurement frequency be low enough to prevent the introduction of the error stemming from parasitic components, and frequencies below 2 MHz are preferred. Therefore, 100 kHz was selected as the measurement frequency.

III. MEASUREMENT OF C–V CHARACTERISTICS

This section certifies the measured capacitance using the developed capacitance measurement circuit, based on a reference capacitance set whose values are known *a priori*. The measured C–V characteristics of an example device are presented and their features discussed as associated with the device structure and composition.

A. Certification of the Measurement Circuit

The developed capacitance measurement circuit is connected to a HIOKI 3522 *LCR* meter to quantify the capacitance through measurement terminals $H_{\rm cur}$, $H_{\rm pot}$, $L_{\rm cur}$, and $L_{\rm pot}$. At the beginning of setting up the experiment, open- and short-circuit

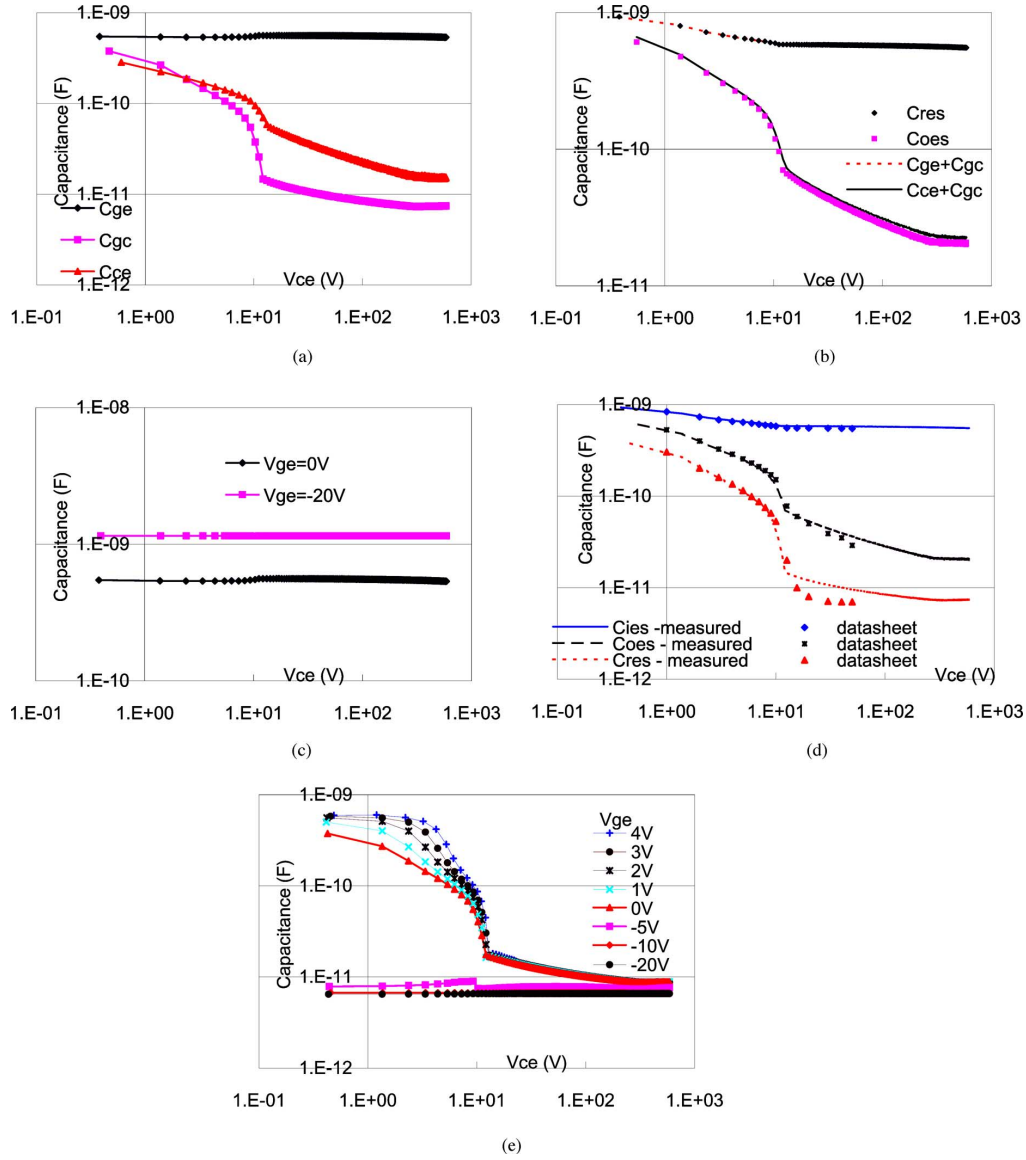

Fig. 8. Measured C–V characteristics for $V_{\rm ce}$. (a) $C_{\rm ge}$, $C_{\rm gc}$, and $C_{\rm ce}$ ($V_{\rm ge} = 0$ V). (b) $C_{\rm ies}$ and $C_{\rm oes}$ ($V_{\rm ge} = 0$ V). (c) $C_{\rm ge}$ for different $V_{\rm ge}$. (d) Comparison between measured value and datasheet. ($V_{\rm ge} = 0$ V). (e) $C_{\rm gc}$ ($C_{\rm res}$) for different $V_{\rm ge}$.

calibration of the measurement circuit is performed for *LCR* meter operation. Although the developed circuit applies a bias voltage between terminals, a dc short-circuit current flows through the bias voltage source. Therefore, a 0-V dc bias voltage is applied during circuit calibration.

Three capacitances *Ca*, *Cb*, and *Cc*, whose values are given in the margin of Table I and are similar to those of an actual semiconductor device, are used to validate the measurement circuit. The test capacitors are connected in delta to imitate the terminal capacitance of a power device, and six possible combinations of the terminal connection are tested for the five capacitance measurements. The measured values for the respective combinations of reference capacitance connections are given in Table I. The relative percentage error of the actual value is also given in parentheses. The compound capacitances $C_{\rm gs} + C_{\rm gd}$ and $C_{\rm ds} + C_{\rm gd}$, which are, respectively, equivalent to $C_{\rm iss}$ and $C_{\rm oss}$, are also shown in the table for comparison.

The measurement errors for $C_{\rm gd}$ and $C_{\rm iss}$ were confirmed as less than 1%—a low error. The error in measuring $C_{\rm gs}$ tends to become large when $C_{\rm ds}$ is larger than $C_{\rm gs}$. This can be attributed to measurement signal leakage in the blocking inductor $L1$ and bypass capacitor $C7$ (see Fig. 2). The opposite effects are found in the measurement of $C_{\rm ds}$. The error in $C_{\rm ds}$ becomes large when $C_{\rm gs}$ is larger than $C_{\rm ds}$. This is attributed to measurement signal leakage in blocking inductor $L1$ and bypass capacitor $C6$ (see Fig. 4). Thus, the errors of compound capacitance $C_{\rm gs} + C_{\rm gd}$ tend to become larger than directly measured $C_{\rm iss}$, except when $C_{\rm ds}$ is small. The error in the measured $C_{\rm oss}$ becomes large when $C_{\rm gd}$ is larger than $C_{\rm ds}$. Leakage of the measurement signal through $L1$ in Fig. 6 cannot explain this phenomenon. Hence, this can be attributed to the residue of the measurement signal for the bypass capacitor $C6$ (see Fig. 6), i.e., the detection terminal for $C_{\rm ds}$ is directly connected to the *LCR* meter through $L_{\rm cur}$ and $L_{\rm pot}$ terminals, but the detection terminal for $C_{\rm gd}$ is

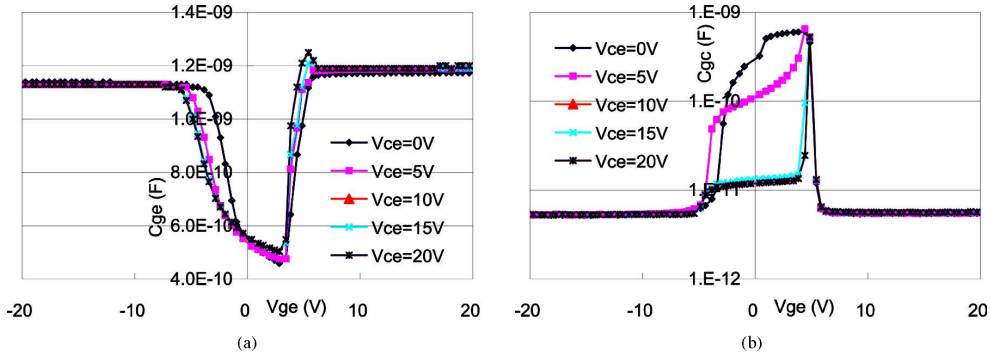

Fig. 9. Measured C–V characteristics for V_{ge}. (a) C_{ge}. (b) C_{gc} (C_{res}).

indirectly connected to the *LCR* meter through $C6$. Therefore, the C_{oss} measurement circuit is amenable to C_{gd} value, and the errors of directly measured C_{oss} tend to become larger than the compound capacitance $C_{\mathrm{ds}} + C_{\mathrm{gd}}$ when C_{gd} is small.

The extracted error falls within 5% using the measurement circuit parameters, as shown in Figs. 2–7. This error can be reduced by increasing the value of the blocking and bypassing elements, but the accuracy given in Table I is sufficient to characterize the device because of the dispersion of the characteristics among devices.

B. Measured Results

The measured C–V characteristics are exemplified here by considering a planar gate IGBT with a 600-V-rated voltage (IRG4BC20S) as an example, and the relationship of the capacitance characteristics to the device structure is discussed.

Fig. 8(a) illustrates the relationship of the measured $C_{\mathrm{ge}}(= C_{\mathrm{gs}})$, $C_{\mathrm{gc}}(= C_{\mathrm{gd}})$, and $C_{\mathrm{ce}}(= C_{\mathrm{ds}})$ to the collector voltage with $V_{\mathrm{ge}} = 0$ V. C_{ge} is larger than C_{ce} and C_{gc} because of the closely spaced gate and emitter electrodes at the surface of the device. It barely changes with the applied V_{ce}, because V_{ce} does not affect the expansion of the depletion region across the gate and emitter. Also, depletion in the drift layer depends on V_{ce}. Therefore, C_{ce} and C_{gc} decrease with increase in V_{ce} in accordance with the expansion of the depletion region. There are irregular capacitance changes around $V_{\mathrm{ce}} = 10$ V, which can be attributed to the transition of the expanding depletion region from the JFET region of the planar gate IGBT to the entire drift region. The decrease of the capacitance in C_{ce} and C_{gc} stops around $V_{\mathrm{ce}} = 300$ V, which indicates the termination of the depletion region expansion in the drift layer because of the punch-through structure of the device.

Fig. 8(b) illustrates the directly measured $C_{\mathrm{ies}}(= C_{\mathrm{iss}})$ and $C_{\mathrm{oes}}(= C_{\mathrm{oss}})$ and the calculated $C_{\mathrm{ies}}(= C_{\mathrm{ge}} + C_{\mathrm{gc}})$ and $C_{\mathrm{oes}}(= C_{\mathrm{ce}} + C_{\mathrm{ge}})$ from the measured C_{ce}, C_{ge}, and C_{gc}. The respective results coincide, validating the adequacy of the measured results. Fig. 8(d) compares the measured $(C_{\mathrm{ies}}, C_{\mathrm{oes}}, C_{\mathrm{res}})$ and datasheet values. The datasheet provides capacitances up to $V_{\mathrm{ge}} = 50$ V and validates the measured capacitances.

Fig. 8(c) shows C_{ge} to V_{ce} for different V_{ge}. The accumulation of charge (holes) occurs at the device channel and results in a decrease in C_{c}, as shown in Fig. 1(a), when a gate voltage of $V_{\mathrm{ge}} = -20$ V is applied. Capacitance C_{ge} becomes larger

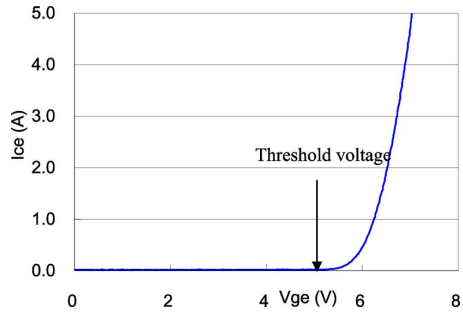

Fig. 10. Measured V_{ge}–I_{ce} characteristics.

than the depleted condition of the channel by the time $V_{\mathrm{ge}} = 0$ V. This phenomenon is shown clearly in Fig. 9(a), where C_{ge} is measured to V_{ge} and V_{ce} is changed as the parameter. Capacitance C_{ge} begins to decrease when V_{ge} becomes higher than -6 V and it reaches a minimum around $V_{\mathrm{ge}} = 3$ V. This indicates the depletion of the accumulated charge (holes) at the channel with increase in gate voltage V_{ge}. The inversion at the channel begins to occur with increasing gate voltages when V_{ge} exceeds 3 V, and C_{ge} increases to the threshold gate voltage. The threshold gate voltage of this device is 5 V, as shown in Fig. 10, and the channel conducts for a higher gate voltage. Fig. 8(e) shows C_{ge} (C_{res}) to V_{ce} for different V_{ge}. The accumulation phenomenon is also seen at the top of the JFET region in a planar device [around C_{gdj} in Fig. 1(a)], and C_{gc} varies with V_{ge} especially in the low V_{ce} region $(V_{\mathrm{ce}} < 10$ V). It also shows that negative V_{ge} reduces C_{gc}. This phenomenon is clearly confirmed in Fig. 9(b), where C_{gc} is measured at V_{ge} and V_{ce} is the parameter being changed. The accumulation at the top of the JFET region tends to occur when voltages with different polarities are applied across that part, resulting in an increase in C_{gdj} [see Fig. 1(c)]. Then, C_{gc} becomes large for low V_{ce} within the -6 V $< V_{\mathrm{ge}} < 3$ V region.

The capacitance measurement is by no means restricted to merely determining the capacitance between terminals, but it can also clarify a wide variety of physical phenomenon occurring in the device.

IV. Conclusion

The capacitances between the terminals of a power device are important in understanding the dynamic behavior of the

device, such as its switching operation. The device capacitances are not constant and change with the voltage applied between the terminals. Therefore, a C–V characterization system for gate-controlled power devices was developed in this study. Five measurement circuits were proposed to measure the three combinations of capacitances between the device terminals, and three combinations of device capacitance for circuit operation. The adequacy of the proposed measurement system was verified using a reference capacitance and the factor of error was discussed. The developed capacitance characterization system can measure capacitance from the blocking condition to the conducting condition while changing the gate bias voltage. The variation of the depletion and accumulation condition in the device was reflected in the device capacitance. The measured capacitance explained the device structure and the physical phenomenon occurring in the device.

ACKNOWLEDGMENT

The authors thank to Prof. J. C. Balda from the University of Arkansas for discussions regarding C–V measurements.

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